ESD Reliability Report

PS081 - QFN56

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Test results of reliability test:

In the following you find the reliabilty report for this device. There is no anomaly and we assure good ESD reliability for this device.

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1.0 INTRODUCTION

The abbreviation ESD stands for Electro Static Discharge. All electronic devices are affected by ESD or static electricity. ESD is caused by a bolt of static charge moving between two insulator surfaces that have different potentials, possibly causing enough current flow to damage oxides, metallisations and junctions. Given the current trend of smaller device dimensions and higher speeds, ESD is becoming an increasingly important issue in the semiconductor industry. It is one major consideration in the design and manufacture of integrated circuits. ESD can have a degrading or destructive effect on all IC s, which is why different standards like Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM) and IEC 61000-4-2 have been developed to test devices for robustness and ensure ESD protection.

The IEC 61000-4-2 standard is a predominantly European norm for ESD testing that aims at ensuring system level ESD testing , i.e. ensuring that finished products at the hands of the end user will withstand high voltage stress due to ESD. The device was tested towards this norm.

The following document gives an account of the ESD tests performed on the PS081 and the observations thereof.

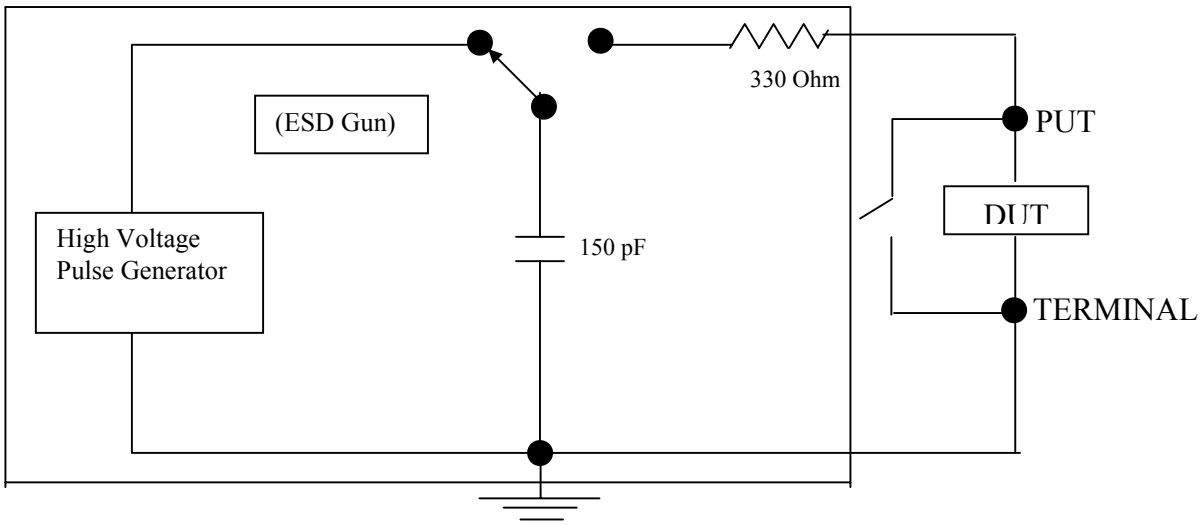
2.1 TEST SETUP

The IEC 61000-4-2 standard is used to certify the ESD reliability of the PS081. This norm defines 4 standard levels of ESD protection, Levels 1, 2, 3 and 4 ; each using 2 different methodologies. The different levels indicate the level of high voltages that the devices can withstand. The two methodologies that can be used are the contact discharge or the air discharge method. In the contact discharge method, the high ESD voltage is discharged to the Device Under Test (DUT) from an ESD gun through actual physical contact of the DUT to the gun tip. In the air discharge method, the ESD test gun is brought close to the DUT until a discharge through the air gap occurs.

For ensuring the ESD reliability in PS081, the contact discharge method is used. The voltages corresponding to the 4 standard levels using the contact discharge method are shown in the table below.

CONTACT DISCHARGE	
Standard Level	Test Voltage in kV
1	2
2	4
3	6
4	8

Block diagram of the ESD testing setup :



Description:

1. The PS081 is the DUT. Some pins of the PS081 are short listed as candidates to be subjected to the ESD test. The selected pin is called **P**in **U**nder **T**est (PUT). These pins are selected based on their ESD protection circuitry and their functionality. Among similar pins like for e.g. the LCD pins, only one or two of the kind are selected.
2. Each PUT is tested by applying the ESD voltage between the selected pin and one of the other pins of the device. This other pin which is indicated as TERMINAL in the block diagram can be a Ground pin or a VCC corresponding to the PUT (the VCC pin located closest to the PUT) or any other pin of the device. The terminal (Ground/VCC/other pin) is connected back to the ESD gun which in turn is grounded.
3. The test voltages have to be applied to the PUT with positive and negative polarity. (See description of the test procedure below)
4. In accordance with the IEC 61000-4-2 standard, the ESD gun discharges the voltage from a 150 pF capacitor through a 330 Ohm resistor. This arrangement is part of the ESD gun itself.
5. The entire ESD testing procedure is carried out in a test setup in compliance with the requirements of the IEC 61000-4-2 standard .
6. The following table shows a list of the pins selected as PUT and their respective VCC pins.

PUT	Respective VCC pin
sense_in	VCC
sense_out	VCC
ucomp1	VCC
ucomp2	VCC
stop	VCC
SG_D1	VCC
SG_B2	VCC
cpump1	VCC_LCD
cpump2	VCC_LCD
cpump3	VCC_LCD
LCD_COM4	VCC_LCD
LCD_SEG07	VCC_LCD
LCD_SEG14	VCC_LCD
LOAD	VCC_LOAD
SPI_DI_IO1	VCC_OSC
OSC_OUT	VCC_OSC
OSC_IN	VCC_OSC
SPI_EN	VCC_OSC

2.1 TEST PROCEDURE

1. A test chip is selected and its quiescent current (Iddq) is measured after inserting the chip into a socket on an evaluation board. Then the chip is tested using the standard test board and software to verify that it is fully functional and operates according to ist product specification.
2. The selected terminal pin of the chip, e.g. VCC, is connected to the feedback connection to the ESD gun. The desired ESD voltage according to the Standard Level 1,2,3 or 4 is set in the gun. The test was first performed with the Level 1 voltage of 2 kV.
3. The ESD voltage with a positive polarity is applied once to the selected PUT by contacting the gun tip with the PUT and pulling the trigger on the ESD gun to apply the discharge voltage.
4. After applying the test voltage to the PUT any residual electric charge is removed by shorting the PUT to ground directly by closing the switch shown between the PUT and the terminal pin in the block diagram.
5. Then the ESD voltage with a negative polarity is applied once to the selected PUT by again contacting the gun tip with the PUT and pulling the trigger on the ESD gun to apply the discharge voltage.
6. Any residual electric charge is removed.
7. The above steps 3 – 6 are performed 3 times.
8. This is the completion of the ESD test itself. The chip is then inserted into the testboard, and its quiescent current is noted again.
9. The complete standard test to verify the functionality and operation of the chip is performed again.

10. The above procedure is repeated for various pins on which the voltage is applied, for various terminal pins, and for various ESD voltages. Conclusions are derived based on the quiescent current measurements and the state of the chip post ESD test.
11. When the pins are tested, every time the quiescent current after the ESD test changes drastically the chip is deemed broken and a new chip is taken for the ensuing tests.

Acceptance criteria:

1. For a chip to be certified as acceptable after being subjected to the ESD test, the quiescent current (Iddq) must be less than or equal to ***1 uA***.
2. Additionally, the chip must be fully functional and operational according to its specifications.

2.3 TEST RESULTS:

Quiescent current before ESD test Iddq = 30 - 60 nA				
Test no	ESD voltage in kV	Quiescent current (Iddq) after ESD test	Pin – Terminal	Measurement current in uA
1	2	65 nA	sense_in – VCC	330
2		55 nA	sense_out – VCC	330
3		50 nA	ucomp1 – VCC	330
4		160 nA	ucomp2 – VCC	330
5		160 nA	stop – VCC	330
6		170 nA	cpump1 – VCC_LCD	330
7		175 nA	cpump2 – VCC_LCD	330
8		380 nA	cpump3 – VCC_LCD	330
9		320 nA	SG_D1 – VCC	330
10		340 nA	SG_B2 – VCC	330
11		40 nA	LCD_COM4 – VCC_LCD	330
12		40 nA	LCD_SEG07 – VCC_LCD	330
13		40 nA	LCD_SEG14 – VCC_LCD	330
14		30 nA	LOAD – VCC_LOAD	330
15		500 nA	SPI_DI_IO1 – VCC_OSC	330
16		610 nA	OSC_OUT – VCC_OSC	330
17		650 nA	OSC_IN – VCC_OSC	330
18		660 nA	SPI_EN – VCC_OSC	330
19		160 nA	sense_in – GND	330
20		160 nA	cpump1 – GND	330
21		160 nA	cpump2 – GND	330
22		350 nA	cpump3 – GND	330
23		35 nA	OSC_IN – GND	330

24		35 nA	OSC_OUT – GND	300
25		30 nA	LCD_COM4 – GND	330
26		30 nA	LCD_SEG07 – GND	330
27		35 nA	LCD_SEG14 – GND	330
28		90 nA	SG_D1 – GND	330
29		100 nA	SG_B2 – GND	330
30		100 nA	SPI_DI_IO1 – GND	330
31		50 nA	SPI_EN – GND	330
32		58 nA	sense_out – GND	330
33		55 nA	ucomp1 – GND	330
34		60 nA	ucomp2 – GND	330
35		60 nA	stop – GND	330
36		65 nA	LOAD – GND	330

The test results displayed in the above table show that every pin of the PS081 can withstand an ESD event voltage of at least level 1 (2 kV) without compromising the functionality and operation of the device or raising the quiescent current (Iddq).

Note : The values stated in the above table are results of tests, in which the pin is subjected to 2kV repeatedly, multiple number of times, before being discharged once. This is more stressful to the chip, than the normal test procedure explained above. Hence the values of the quiescent currents are higher than what would be obtained by the normal test procedure.

2.4 TEST OF INTERFACE PINS:

The interface pins on any chip that come in contact with the outside world and the end user after the chip has been mounted to a consumer product are the most crucial pins in terms of ESD reliability because they are the most probable targets for ESD. Additionally there are certain pins like the LCD pins that could be subjected to ESD during the assembly of the board or device. Hence the level of ESD resistance of these pins must be higher and they are tested for higher ESD voltages. For the PS081, the interface pins include the port pins that are connected to the load cell, the SPI Interface pins and the LCD pins. The following is a list of interface pins that were selected and subjected to higher ESD voltages:

1. SG_D1
2. SG_B2
3. LOAD
4. SENSE_IN
5. SPI_DI_IO1
6. SPI_EN
7. LCD_COM4
8. LCD_SEG07
9. MULT_IO3

The following are the test results for the interface pins with higher ESD voltages:

1. All the above mentioned interface pins were subjected to voltages from 2kV to 8kV, the voltage level was increased in 1000 V steps. The pins were tested against their respective VCC.
2. All the port pins including the LOAD and SENSE_IN can safely withstand a voltage of 8kV without causing any damage to the quality of operation of the chip and without significantly affecting the Iddq of the chip.
3. The pins of the SPI interface can also safely withstand an ESD voltage as high as 8kV without causing any damage to the quality of operation of the chip and without significantly affecting the Iddq of the chip.
4. The LCD pins were also tested for higher voltages. These pins fail to function properly when subjected to a voltage stress of 6 kV, though the quiescent current is not altered very much. Hence all the LCD pins can be specified to be safely functional, till a maximum ESD voltage of 4 kV.
5. It is observed that the resulting Iddq for all the tested pins, for the specified voltage level, is always less than 1 uA after the ESD tests.

Note: The above set of pins is not a complete list of interface pins. The underlying ESD circuitry in the IO Buffers of certain sets of pins are identical. Hence such pins will react to ESD in a similar manner. So not all the pins were explicitly tested, but one or two were chosen from each set of similar pins.

From the load cell port pins, the SG_D1 and SG_B2 were selected. From the digital pins, SPI_DI_IO1 and SPI_EN were selected. From the LCD pins, the LCD_COM4 and LCD_SEG07 were selected. From the IO pins, the MULTIO3 pin was chosen.

The following table summarises the results of all the tests performed above:

Pin Number	Pin Name	Tested against	Tolerable tested ESD Voltage	Remarks
1	GND			
2	Vcc			
3	**SG_D1**	**VCC (Pin 2)**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
4	SG_D2	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages. Not tested directly, ESD circuit similar to Pin 3
		GND		
5	SG_C1	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 3
		GND		
6	SG_C2	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 3
		GND		
7	SG_B1	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 3
		GND		
8	**SG_B2**	**VCC (Pin 2)**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
9	SG_A1	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 8
		GND		
10	SG_A2	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 8
		GND		
11	PSEP1	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 8
		GND		

12	PSEP2	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 8
		GND		
13	MULT_IO5	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 26
		GND		
14	GND			
15	MULT_IO4	VCC (Pin 2)	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 26
		GND		
16	Vcc_load			
17	**Load**	**VCC_LOAD**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
18	SPI_DO_IO0	Vcc_OSC	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 19
		GND		
19	**SPI_DI_IO1**	**Vcc_OSC**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
20	SPI_CLK_IO2	Vcc_OSC	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 19
		GND		
21	OSC_OUT	Vcc_OSC	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 19
		GND		
22	OSC_IN	Vcc_OSC	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 19
		GND		
23	VCC_OSC			
24	SPI_CSN_RST SPI_SSN_RST	Vcc_OSC	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 25
		GND		
25	**SPI_ENA**	**Vcc_OSC**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
26	**MULT_IO3**	**Vcc_OSC**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
27	Vcc			
28	GND			
29	Vcc			
30	**SENSE_IN**	**VCC (Pin 29)**	**8 kV**	
		GND	2 kV	Not tested for higher ESD voltages
31	SENSE_OUT	Vcc_OSC	2 kV	Not tested for higher ESD voltages
		GND		
32	UCOMP1	Vcc_OSC	2 kV	Not tested for higher ESD voltages
		GND		
33	UCOMP2	Vcc_OSC	2 kV	Not tested for higher ESD voltages
		GND		
34	STOP	Vcc_OSC	2 kV	Not tested for higher ESD voltages
		GND		
35	VCC_LCD			
36	CPUMP1	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		
37	CPUMP2	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		
38	CPUMP3	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		
39	LCD_COM1	VCC_LCD	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 42
		GND		
40	LCD_COM2	VCC_LCD	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 42
		GND		
41	LCD_COM3	VCC_LCD	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 42
		GND		

42	**LCD_COM4**	**VCC_LCD**	**4 kV**	
		GND	2 kV	Not tested for higher ESD voltages
43	**LCD_SEG01**	**VCC_LCD**	**4 kV**	
		GND	2 kV	Not tested for higher ESD voltages
44	LCD_SEG02	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 43
45	LCD_SEG03	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 43
46	LCD_SEG04	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 43
47	LCD_SEG05	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 43
48	LCD_SEG06	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 43
49	**LCD_SEG07**	**VCC_LCD**	**4 kV**	
		GND	2 kV	Not tested for higher ESD voltages
50	**LCD_SEG08**	**VCC_LCD**	**4 kV**	
		GND	2 kV	Not tested for higher ESD voltages Not tested directly, ESD circuit similar to Pin 49
51	LCD_SEG09	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 49
52	LCD_SEG10	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 49
53	LCD_SEG11	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 49
54	LCD_SEG12	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 49
55	LCD_SEG13	VCC_LCD	2 kV	Not tested for higher ESD voltages
		GND		Not tested directly, ESD circuit similar to Pin 49
56	**LCD_SEG14**	**VCC_LCD**	**4 kV**	
		GND	2 kV	Not tested for higher ESD voltages

3.0 CONCLUSION:

The results obtained in this reliability test show that every pin of the PS081 can withstand an ESD event voltage of at least level 1 (2 kV) without compromising the functionality and operation of the device or raising the quiescent current (Iddq). Crucial pins in the sense of being most likely exposed to ESD influences, such as LCD or interface pins were tested additionally against level 2 (4kV) and 3 (6kV) with good results showing a quiescent current of less than 1 µA consistently after ESD. The LCD pins can be specified safely to level 2 and the SPI interface pins to level 3. The port pins resist even to level 4 (8kV) without causing any damage to the quality of operation of the chip and without significantly affectiong the Iddq of the chip.